

CUSTOMER NO. 23932

PATENT APPLICATION  
Docket No. 61180-6USPX

**IN THE DRAWINGS:**

Replacement sheets for Figures 1 and 2 are attached hereto. These replacement sheets amend previously submitted Figures 1 and 2 to include a "Prior Art" legend.

**REMARKS**

New claims 26-31 have been added. Claims 1-9 and 22-31 are now pending in the application.

The Examiner notes that the priority document has not yet been submitted. Applicant will file the priority document in the near future.

Figures 1 and 2 of the application have been amended to include a "Prior Art" legend. Appropriate replacement sheets are submitted herewith.

Claims 1-9 have been allowed. Claim 25 has been objected to as being dependent on a rejected base claim. Claim 25 has been amended to include the limitations of independent claim 22, and thus is now in condition for favorable action and allowance (along with new dependent claims 26-27).

Claims 22-24 are rejected under 35 U.S.C 102(a) as being anticipated by Prior Art Figure 2 of the application.

Claim 22 has been amended to emphasize that the selection circuit selectively connects one or more of the first and second plurality of current generators to the analog current output based on a combination of the less significant bit portion and the more significant bit portion of the input digital signal. There is no teaching or suggestion in Prior Art Figure 2 for this claimed feature. If the first current generators are transistors MD1 and MD2, and if the second current generators are transistors MD3 and MD0, as is asserted by the Examiner, it will be noted from Figure 2 that selection circuit SD0-SD2 is controlled responsive to signals SD<2:0>, which are signals generated by TRANSCOD-3BIT solely from the less significant bits D<2:0>. Figure 2

does not teach using D<2:0> AND D<11:3> to generate the selection control signals SD<2:0>.

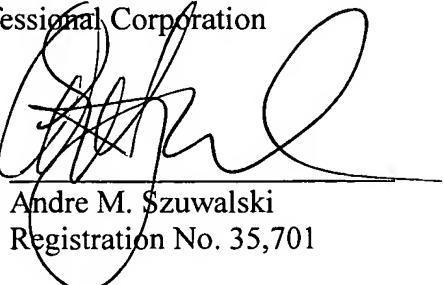
Applicant accordingly submits that claims 22-24 are allowable over the art of record.

Claim 28 recites a first plurality of current generators with a first selection circuit operable to selectively connect one or more of the first plurality of current generators to source current to the analog current output based at least in part on the less significant bit portion of the input digital signal, and a second plurality of current generators with a second selection circuit operable to selectively connect one or more of the second plurality of current generators to sink current from the analog current output based at least in part on the less significant bit portion of the input digital signal. The Prior Art Figure 2 does not teach sourcing and sinking current generators selectively controlled as claimed. Rather, in Figure 2 only sinking current generators MD0-MD2 are shown. Applicant accordingly submits that claims 28-31 are allowable over the art of record.

In view of the foregoing, Applicants respectfully submit that the application is in condition for favorable action and allowance.

Respectfully submitted,  
JENKENS & GILCHRIST,  
A Professional Corporation  
Suite

By:

  
Andre M. Szuwalski  
Registration No. 35,701

1445 Ross Avenue, Suite 3700  
Dallas, Texas 75202-2799  
Tel: 214/855-4795  
Fax: 214/855-4300